REMARKS

Applicant has amended the specification to incorporate the appropriate U.S. Patent Application numbers and remove all references to attorney docket numbers.

Claims 5 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shulholm, U.S. Patent No. 6,104,997 (hereafter referred to as Shulholm '997), in view of Shulholm et al, U.S. Patent No. 5,923,710 (hereafter referred to as Shulholm '710).

The present invention, as defined in amended claim 5, is concerned with a routing switch for connection to a plurality of signal sources. The signal sources each provide a data stream composed of a succession of frames and each frame has first and second subframes. Each subframe includes multiple payload data bits and a data block bit and the first subframe includes framing bits. The succession of first subframes constitutes a first channel and the succession of second subframes constitutes a second channel. The routing switch includes a plurality of input modules (designated 14 in the embodiment shown in FIG. 3) having respective input terminals for connection to the signal sources and a plurality of output modules (designated 58) each having an output terminal for connection to a signal destination. The selected output module (58) includes a circuit which selectively delays the data block bits of the selected channel of the first data stream to bring the data block bits of the selected channel into phase alignment with the data block bits of the selected channel of the second data stream. The routing switch also includes a routing core (54) for supplying selectively a channel of a first data stream and a channel of a second data stream to any selected output module (58) for combination to provide the output data stream.

The present invention, as defined in amended claim 6, is concerned with a method of processing first and second data streams each composed of a succession of frames, each frame having first and second subframes wherein the succession of first subframes constitutes a first channel and the succession of second subframes constitutes a second channel. Each subframe includes multiple payload data bits and a data block bit and the first subframe includes a framing character having a first state to indicate the start of a sequence of data block bits and otherwise having a second state. The method comprises composing an output data stream from a channel of the first data

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stream and a channel of the second data stream and delaying the data block bits of the selected channel of the first data stream relative to the payload data bits of the selected channel of the first data stream to bring the data block bits of that channel into phase alignment with the data block bits of the selected channel of the second data stream.

Shulholm '997 discloses a digital audio receiver with multi-channel swapping capability. Two (or more) AES streams are each received by a respective decoder 12, 13 which extract a clock and two channels of audio data from each stream. Each channel of audio data is then written to a respective synchronizing FIFO 14, 15, 16, 17 using the extracted clock for synchronization. Selectors 20, 22 read out the contents of the FIFOs 14-17 and, based on user input, assign the audio channel data to any channel position within any available AES output. The examiner has acknowledged that Shulholm '997 does not disclose Aa circuit which selectively delays the data block bits of one channel to the data block bits of the one channel to bring into phase alignment with the data block bits of the other channels.

The examiner has asserted that Shulholm '710 discloses selectively delaying the data block bits of one channel to bring them into phase alignment with the data block bits of the other channel. However, the definition of the word "channel" is not consistent between Shulholm '710 and claims 5 and 6 of the present application. The word "channel" is used by the AES Standard for Digital Audio (AES3-2003) to refer to an audio signal represented by the succession of first sub-frames or the succession of second sub-frames, two interleaved "channels" making up a single complete AES audio stream. For example, in a system with separate right (R) and left (L) channels, the R channel could be represented by the succession of first subframes and the L channel could be represented by the succession of second subframes. This definition is consistent with that used by claims 5 and 6 of the present application and by Shulholm '997. Contrastingly Shulholm '710 uses "channel" to describe a complete AES audio stream that is made up of a series of blocks which comprise a series of frames which contain the audio data and auxiliary data of two sub-frames. This is demonstrated by INPUT AES DATA CHANNEL 1 and CHANNEL N in FIG. 2 of Shulholm '710. For clarity, a "channel"

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of Shulholm '710 will hereafter be referred to as an AES audio streams.

Shulholm '710 discloses a system and method for synchronous switching of digital audio while maintaining block alignment. The system contains N AES receiver/separator subsystems as shown in FIG. 1A and one transmittal subsystem as shown in FIG 1B. Each receiver/separator subsystem receives one AES audio stream into a receiver 12, which extracts a recovered clock from the input AES audio stream. The input AES audio stream is then transmitted to a block start detector 18 and a separator 14. The separator 14 separates the status/user bits from the audio data. The status/user bits are then sent to auxiliary FIFO 16 and the audio data is sent to data FIFO 19. The block start detector 18 monitors the input AES audio stream for the status/user bits and enables the input and output of the auxiliary FIFO 16 in conjunction with the recovered clock and a system clock respectively. The system clock also controls the output of the data FIFO 19. When the start of a new block is signaled by the presence of the Z preamble in the input AES audio stream, the block start detector 18 also transmits a reset signal to the transmittal subsystem.

The transmittal subsystem receives the output of all N auxiliary and data FIFOs as well as the reset signals from the N block start detectors. The outputs of the auxiliary FIFOs connect to a status/user multiplexer 26 and outputs of the data FIFOs connect to a data multiplexer 28. The select lines of these multiplexers connect to a controller 24, which is where the block start detector's reset signals are routed. The status/user multiplexer 26 and the data multiplexer 28 connect to a transmitter 30 that combines the status and user bits received from the status/user multiplexer with the audio data received from the data multiplexer to create a valid output AES audio stream.

The blocks of the output AES audio stream are not necessarily aligned with the blocks of any of the N input AES audio streams. Consequently when a user wants to change which AES audio stream is being transmitted from the system, for example from AES audio stream 1 to AES audio stream N, there must be some type of control in place to prevent data being carried by the status and user bits of the AES audio streams from being lost. Shulholm '710 discloses the user input select signal indicating to the controller which AES audio stream the user wants to switch to. At the next instance of the system frame

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start signal indicating the start of a new frame, the controller will
switch the data multiplexer 28 from AES audio stream 1 to AES audio
stream N. However, in order to prevent the aforementioned loss of data
being conveyed by the status and user bits in the current block,
caused by switching between AES audio streams mid-block, the
controller will wait until the system block start signal indicates the
start of a new block before the status/user multiplexer's output is
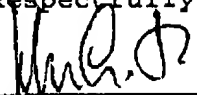changed from AES audio stream 1 to AES audio stream N.

Applicant submits that Shulholm '710 discloses delaying the
transmission of an AES audio stream's status and user bits to bring
them into block alignment with the status and user bits of another AES
audio stream. Applicant believes that the examiner has been misled by
the inconsistency in terminology between Shulholm '997 and Shulholm
'710. Applicant believes that, in view of the clarifications made
regarding the terminology of Shulholm '710 in the preceding
paragraphs, the examiner will recognize the lack of any teaching in
Shulholm '710 toward a circuit which selectively delays the data block
bits of one channel of a selected first data stream (such as an AES
audio stream) to bring the data block bits of the one channel into
phase alignment with a channel of a selected second data stream.

Applicant therefore submits that Shulholm '997 and Shulholm '710,
whether taken singly or in combination, do not disclose or suggest a
routing switch which comprises a circuit which selectively delays the
data block bits a selected channel of a first data stream to bring the
data block bits of the selected channel into phase alignment with the
data block bits of a selected channel of a second data stream.
Therefore, applicant submits that amended claim 5 is patentable over
Shulholm '997 in view of Shulholm '710. Furthermore, Shulholm '997 and
Shulholm '710, whether taken singly or in combination, do not disclose
or suggest a method of processing first and second data streams
wherein the method comprises delaying the data block bits of a
selected channel of a first data stream relative to the payload data
bits of the selected channel to bring the data block bits of the
selected channel into phase alignment with the data block bits of a
selected channel of a second data stream. Therefore, applicant submits

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that amended claim 6 and dependent claim 7 are also patentable over Shulholm '997 in view of Shulholm '710.
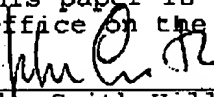
Respectfully submitted,

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